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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,420	09/25/2003	Hiroshi Iwasaki	242393US-2 DIV	5064

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
CHACE, CHRISTIAN	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,420	IWASAKI, HIROSHI	
	Examiner	Art Unit	
	Christian P. Chace	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-17 and 31-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-17* is/are rejected.

7)☒ Claim(s) *31-52* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/457,524.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/25/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action has been issued in response to preliminary amendment filed 25 September 2003. Claims 13-17 and 31-52 are pending.

Information Disclosure Statement

IDS submitted 25 September 2003 has been considered by examiner, with the exception of the Japanese document cited – it was not scanned if it was received by the Office. Accordingly, a line has been drawn through it and it has not been considered. A signed and initialed copy is attached hereto.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13-14 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki (US Patent 5,550,709) in view of Takahira (US Patent 4,960,982).

With respect to independent claims 13 and 16, Iwasaki discloses a semiconductor element mounted on the first face of a wiring board in column 3, lines 42-45, e.g. A resin seal for covering the first face of the wiring board and the semiconductor element is disclosed in column 3, lines 38-40, e.g. A wiring board having first and second faces is inherent.

The difference between the external storage device of Iwasaki and the claims are the explicit disclosure of the security functions as claimed (and will be addressed below).

Takahira discloses the semiconductor element having a first memory area (figure 1, #3), a second memory area (figure 1, #4), first wiring for controlling data write and erase operations of the first memory area (inherent in a printed circuit board, e.g., traces, etc.), a first terminal for controlling the first wiring (in figure 1, connection between #2 and #3), second wiring for controlling a data write operation of the second memory area (again inherent), and a second terminal for controlling the second wiring (in figure 1, half of the connection between #4 and #7).

Takahira also discloses an external terminal arranged on the second face of the wiring board, connected to the second terminal, and electrically separated from the first terminal in figure 1, which is the half of the connection between #4 and #7 that is touching #7.

Takahira also discloses certification data that is unique to the semiconductor element, stored in the first memory area in figure 3, #11, #12, #10, e.g.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Iwasaki and Takahira before him/her, to utilize the security system of Takahira in the card of Iwasaki, because it provides security equivalent to microprocessor controlled cards, and provides on the credit card security means for guarding the information recorded in the mass storage memory, e.g., as discussed in column 1, lines 53-65.

With respect to claim 14, a circuit which controls a conducting state arranged between the first terminal and the first wiring is disclosed by Takahira as #2 in figure 1, e.g.

With respect to claim 17, a module which integrates the semiconductor element, external terminal, resin, and a card-type support which supports the module is disclosed by Iwasaki in column 4, line 16, e.g.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Iwasaki and Takahira as applied to claims 13-14 and 16-17 above, and further in view of Microsoft Press Computer Dictionary, page 163, 1993 (herein after MPCD).

The claims upon which the instant claim depends are disclosed as discussed supra with respect to same.

The difference between the instant claim and the combination as discussed supra is a transistor being arranged between the first memory area and the first wiring, a gate electrode of the transistor being connected to the first terminal.

Having some sort of switch between the memory and the means for outputting the data in the memory (in this case the wiring) is inherent – there must be some sort of switch to let the data pass from the memory at the required time, and not let all the data in the memory pass out all at once, e.g.

MPCD discloses that a FETs are used as switches on page 163.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Iwasaki, Takahira, and MPCD before

him/her, to utilize the FET of MPCD as the switch in the system of Takahira and Iwasaki, because FETs are characterized by an extremely high input impedance that makes them particularly suitable for amplification of very small signals [such as data from a memory, especially when one wishes, as in an IC card design, to use as little power as possible], as discussed in MPCD on page 163.

Allowable Subject Matter

Claims 31, 35, 36, 42, and 46 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

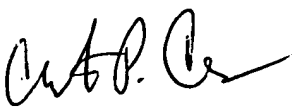
Accordingly, claims 32-34, 37-41, 43-45, and 47-52 depend upon one of the respective claims objected to supra, and would be allowable for at least the same reasons as those claims upon which they depend.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian P. Chace whose telephone number is 571.272.4190. The examiner can normally be reached on MAXI FLEX.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571.272.4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Christian P. Chace
Primary Examiner
Art Unit 2189